Amendments to the Abstract:

Please substitute the following version of the Abstract, with changes shown by strikethrough (for deletions) or underlining (for added matter).

ABSTRACT OF THE DISCLOSURE

A device for the emulation of designs for integrated circuits having a receiving device ~~(1, 2, 3, 4, 5, 6)~~ for multiple programmable logic circuits ~~(11, 12, 13; 21, 22, 23)~~, particularly FPGAs, and an electrical connection structure ~~(14; 24)~~;. The interconnection structure ~~which~~ has bus lines ~~(111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232)~~, each of which includes multiple channels ~~(1...k)~~;. The interconnection structure is configured so ~~is distinguished in~~ that each programmable logic circuit ~~(11, 12, 13; 21, 22, 23)~~ is connected to at least one bus line ~~(111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232)~~ and the connection structure ~~(14; 24)~~ is implemented so it ~~may~~ can be flexibly interconnected, ~~in that~~ wherein the assignment of at least a part of the terminal contacts of any programmable logic circuit ~~(11, 12, 13; 21, 22, 23)~~ is freely programmable and ~~in that~~ wherein at least a part of the bus lines ~~(111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232)~~ connected to the programmable logic circuits ~~(11, 12, 13; 21, 22, 23)~~ are alternately electrically connectable to one another in such a way that at least one channel ~~(1...k)~~ of a bus line ~~(111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232)~~ is electrically connectable to a channel ~~(1...k)~~ of at least one other bus line ~~(111, 112, 121, 122, 131, 132; 211, 212, 221, 222, 231, 232)~~ using a switch ~~(S_1...S_k)~~.

~~(Figure 3 for this purpose)~~